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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,603	02/11/2004	Michael Hutton	306812005800	4958

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BEYER WEAVER & THOMAS, LLP
ATTN: ALTERA
P.O. BOX 70250
OAKLAND, CA 94612-0250

EXAMINER	
CHO, JAMES HYONCHOL	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 08/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/777,603	HUTTON ET AL.	
	Examiner	Art Unit	
	James Cho	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-12 and 14-20* is/are rejected.

7)☒ Claim(s) *8,13 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to because lines, numbers & letters in Figs. 1-5 are not uniformly thick and well defined, clean, durable, and black. 37 CFR 1.84(l). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

Claims 1, 2, 5, 11, and 18 are objected to because of the following informalities:

"signal lines" on line 7 of claim 1 appears to be --first signal lines--;

"swap" on line 8 of claim 2, on line 5 of claim 5, on line 5 of claim 11 and on line 7 of claim 18 appears to be --first swap-- respectively.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-7, 9-12 and 14-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Lytle et al. (US PAT No. 6,492,834).

Regarding claims 1 and 14, Fig. 6 of Lytle et al. teaches a programmable logic device (PLD) and a method of driving logic array blocks (LABs) in a PLD including: at least first and second logic array blocks, LABs (LAB comprising a column of LE 300 on

the left side, first LAB, hereinafter, LAB comprising a column of LE 300 on the right side, second LAB, hereinafter); a plurality of first signal lines capable of driving the second LAB (signal lines driving the second LAB including 504); a plurality of output lines (output lines of the first LAB) driven by the first LAB; and a first swap multiplexer, MUX (INPUT MUX REGION 504 on the left side, MUX, hereinafter) having a first selectable input capable of being driven by at least one of the plurality of output lines (504 on the left side, MUX hereinafter, receives inputs from the outputs from LEs of the first LAB) and a second selectable input capable of being driven at least one of the plurality of first signal lines (first signal lines driving second LAB coupled to MUX via GH210), and an output capable of driving the at least first LAB (outputs of MUX drives LEs of the first LAB).

Regarding claims 2 and 15, Fig. 6 of Lytle et al. teaches the PLD of claim 1 and the method of claim 14 wherein: the first LAB includes a first plurality of logic elements (LEs 300) and the second LAB includes a second plurality of LEs (first and second LAB comprising LEs 300); at least one of the plurality of output lines is driven by at least one of the first plurality of LEs (output of LEs of first LAB driving respective output lines); at least one of the plurality of first signal lines is capable of driving at least one of the second plurality of LEs (LEs of the second LAB are driven by the first signal lines); and the output of the first swap MUX is capable of driving at least one of the first plurality of LEs (output of MUX drives LEs of first LAB).

Regarding claims 3 and 16, Fig. 6 of Lytle et al. teaches the PLD of claim 2 and the method of claim 15 wherein the first LAB includes a plurality of local lines at least one of which drives at least one of the first plurality of LEs (lines coupled to inputs of LEs of the first LAB) and the output of the first swap MUX drives at least one of the plurality of local lines (local lines coupling output of MUX to inputs of LEs of the first LAB).

Regarding claims 4 and 17, Fig. 6 of Lytle et al. teaches the PLD of claim 3 and the method of claim 16 further including at least one additional signal line for exclusively driving the second LAB (signal lines coupling the outputs of LEs of the second LAB to 504 which drives the input of LEs of the second LAB).

Regarding claims 5 and 18, Fig. 6 of Lytle et al. teaches the PLD of claim 4 and the method of claim 17 wherein the plurality of first signal lines include a plurality of LAB lines which drive the second LAB (inputs of LEs of the second LAB driven by lines from 504) and a plurality of tap lines at least one of which is interconnected with at least one of the plurality of LAB lines (part of GH210 interconnected with input lines of LEs via 504), at least one of the plurality of tap lines driving the first selectable input of the first swap MUX (part of GH 210 connected to the inputs of MUX).

Regarding claims 6 and 19, Fig. 6 of Lytle et al. teaches the PLD of claim 5 and the method of claim 18 wherein the interconnection between the at least one LAB line and at least one tap line is fixed (when 504 is selectively set, the connection from GH210 to inputs of LEs of the second LAB is fixed).

Regarding claims 7 and 20, Fig. 6 of Lytle et al. teaches the PLD of claim 6 and the method of claim 19, Fig. 8 of Lytle et al. further includes at least a third LAB and a plurality of second signal lines (signal lines for the bottom LAB 200) capable of driving the third LAB where the first swap MUX includes a third selectable input and at least one of the second signal lines drives the third selectable input (inputs of IMR 504 being coupled to a third LAB 200 via GV220 and programmable connection 808).

Regarding claim 9, Fig. 6 of Lytle et al. teaches a programmable logic device (PLD) including: at least first and second logic array blocks, LABs (LAB comprising a column of LE 300 on the left side, first LAB, hereinafter, LAB comprising a column of LE 300 on the right side, second LAB, hereinafter); at least first and second logic array blocks (LABs), the first LAB including a first plurality of logic elements (LEs 300) and the second LAB including a second plurality of LEs (first and second LAB comprising LEs 300); a plurality of first signal lines capable of driving at least one of the second plurality of LEs (signal lines driving LEs of the second LAB including 504); a plurality of output lines (output lines of the first LAB) driven by at least one of the first plurality of LEs; and a first swap multiplexer, MUX (INPUT MUX REGION 504 on the left side, MUX, hereinafter) having a first selectable input capable of being driven by at least one of the plurality of output lines (504 on the left side, MUX hereinafter, receives inputs from the outputs from LEs of the first LAB) and a second selectable input capable of being driven at least one of the plurality of first signal lines (first signal lines driving second LAB coupled to MUX via GH210), and an output capable of driving the at least first LAB (outputs of MUX drives LEs of the first LAB).

Regarding claim 10, Fig. 6 of Lytle et al. teaches the PLD of claim 9 wherein the first LAB includes a plurality of local lines which drives the first plurality of LEs (lines coupled to inputs of LEs of the first LAB) and the output of the first swap MUX drives at least one of the plurality of local lines (local lines coupling output of MUX to inputs of LEs of the first LAB).

Regarding claim 11, Fig. 6 of Lytle et al. teaches the PLD of claim 10 wherein the plurality of first signal lines include a plurality of LAB linesat least one of which drives the second LAB (inputs of LEs of the second LAB driven by lines from 504) and a plurality of tap lines at least one of which is interconnected with at least one of the plurality of LAB lines (part of GH210 interconnected with input lines of LEs via 504), at least one of the plurality of tap lines driving the first selectable input of the first swap MUX (part of GH 210 connected to the inputs of MUX).

Regarding claim 12, Fig. 6 of Lytle et al. teaches the PLD of claim 11, Fig. 8 of Lytle et al. further includes at least a third LAB and a plurality of second signal lines (signal lines for the bottom LAB 200) capable of driving the third LAB where the first swap MUX includes a third selectable input and at least one of the second signal lines drives the third selectable input (inputs of IMR 504 being coupled to a third LAB 200 via GV220 and programmable connection 808).

Allowable Subject Matter

Claims 8, 13 and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Although Lytle et al. teaches a PLD with highly routable interconnect, one of ordinary skill in the art would not have been motivated to modify the teaching of Lytle et al. to further includes, among other things, the specifics of the plurality of tap lines include a first set of tap lines and a second set of tap lines, at least one of the first set of tap lines capable of driving the first selectable input of the first swap MUX and at least one of the second set of tap lines capable of driving the second selectable input of the second swap MUX (claims 8, 13, 21).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

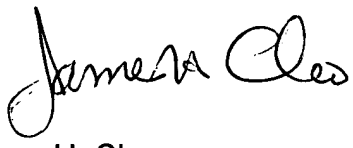
Ngai et al. (US PAT No. 6,614,261) discloses interconnection and input/output resources for programmable logic integrated circuit devices.

Mendel (US PAT No. 6,184,710) discloses programmable logic array devices with enhanced interconnectivity between adjacent logic regions.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Cho whose telephone number is 571-272-1802. The examiner can normally be reached on Monday-Friday 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on 571-272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



James H. Cho
Primary Examiner
Art Unit 2819